19-2448; Rev 0; 4/02

MAXIM

Triple-Output Power-Management IC for Microprocessor-Based Systems

General Description

The MAX1702B power-management IC supports ARM Powered® devices such as the Intel® PXA210 and PXA250 microprocessors based on the Intel XScale™ micro-architecture. These devices include PDAs, third-generation smart cellular phones, internet appliances, automotive in-dash Telematics systems, and other applications requiring substantial computing and multimedia capability at low power.

The MAX1702B integrates three ultra-high-performance power supplies with associated supervisory and management functions. Included is a step-down DC-DC converter to supply 3.3V I/O and peripherals, a step-down DC-DC converter to supply 0.7V to V_{IN} for the microprocessor core, and a step-down DC-DC converter to supply either 1.8V, 2.5V, or 3.3V to power the memory.

Management functions include automatic power-up sequencing, power-on-reset and manual reset with timer, and two levels of low-battery detection.

The DC-DC converters use fast 1MHz PWM switching, allowing the use of small external components. They automatically switch from PWM mode under heavy loads to skip mode under light loads to reduce quiescent current and maximize battery life. The input voltage range is from 2.6V to 5.5V, allowing the use of three NiMH cells, a single Li+ cell, or a regulated 5V input. The MAX1702B is available in a tiny 6mm x 6mm, 36-pin QFN package and operates over the -40°C to +85°C temperature range.

Applications

PDA, Palmtop, and Wireless Handhelds

Third Generation Smart Cell Phones

Internet Appliances and Web Books

Automotive In-Dash Telematics Systems

Typical Operating Circuit appears at end of data sheet.

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XScale is a trademark of Intel Corporation.

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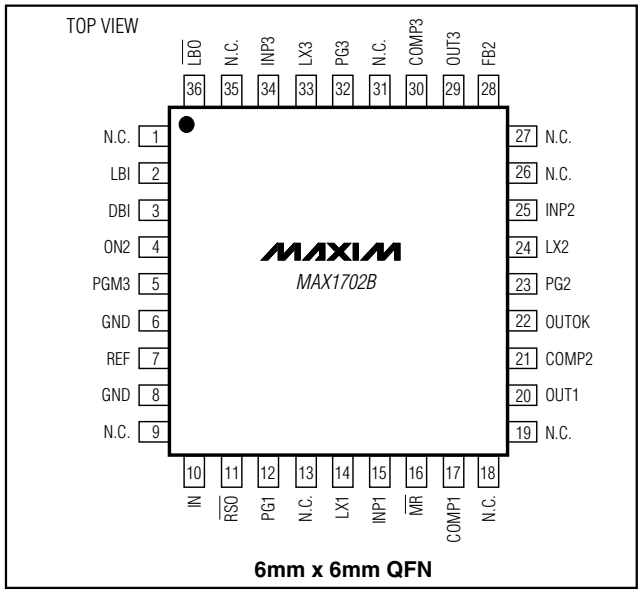
Features

- **Three Regulators in One Package**
  Peripherals and I/O Supply: 3.3V at 900mA
  µP Core Supply: 0.7V to V_{IN} at 400mA
  Memory Supply: 1.8/2.5/3.3V at 800mA
- **Supports Intel PXA210 and PXA250 Microprocessors**
- **Power-On Reset with Manual Reset Input**
- **Auto Power-Up Sequencing**
- **1MHz PWM Switching Allows Small External Components**
- **Low 5µA Shutdown Current**
- **Tiny 6mm × 6mm, 36-Pin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1702BEGX	-40°C to +85°C	36 6mm x 6mm QFN

Pin Configuration



6mm x 6mm QFN

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ABSOLUTE MAXIMUM RATINGS

IN, FB2, OUT3, COMP1, COMP2, COMP3, PGM3, ON2, LBO, OUTOK, RSO, MR, LBI, DBI, OUT1 to GND ..... -0.3V to +6V
REF to GND ..... -0.3 to (V_{IN} + 0.3V)
INP1, INP2, INP3 to IN ..... -0.3V to +0.3V
PG1, PG2, PG3 to GND ..... -0.3V to +0.3V
LX1, LX2, LX3 Continuous Current ..... -1.5A to +1.5A
INP1 to PG1 ..... -0.3V to +6V
INP2 to PG2 ..... -0.3V to +6V
INP3 to PG3 ..... -0.3V to +6V
Output Short-Circuit Duration ..... Infinite
Continuous Power Dissipation (T_A =+70°C)
36-Pin QFN (derate 22.7 mW/°C) 1818mW
Operating Temperature Range ..... 40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{INP1} = V_{INP2} = V_{INP3} = V_{IN} = 3.6V, V_{LBI} = 1.1V, V_{DBI} = 1.35V, $\overline{MR}$ = ON2 = IN, PGM3 = GND, circuit of Figure 1, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INP1, INP2, INP3, IN Supply Voltage Range	INP1, INP2, INP3, IN must be connected together externally	2.6		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising	2.25	2.40	2.55	V
	V_{IN} falling	2.2	2.35	2.525	
Quiescent Current (I_{INP1} + I_{INP2} + I_{INP3} + I_{IN})	ON2 = IN, no load		485		µA
	ON2 = GND, no load		335		
	V_{DBI} < 1.2 V (shutdown) LX1-3 = GND		5	20	
SYNCHRONOUS BUCK PWM REGULATOR 1 (REG1)					
OUT1 Voltage Accuracy	3.6V ≤ V_{INP1} ≤ 5.5V, load = 0 to 900mA	3.234	3.3	3.366	V
OUT1 Input Resistance		200	400		kΩ
Error-Amp Transconductance		55	95	135	µS
Dropout Voltage	Load = 800mA (Note 1)		250	425	mV
P-Channel On-Resistance	I_{LX1} = 180mA		0.25	0.4	Ω
	I_{LX1} = 180mA, V_{INP1} = 2.6V		0.3	0.5	
N-Channel On-Resistance	I_{LX1} = 180mA		0.2	0.35	Ω
Current-Sense Transresistance		0.40	0.47	0.54	V/A
P-Channel Current-Limit Threshold		1.15	1.275	1.45	A
P-Channel Pulse-Skipping Current Threshold		0.115	0.140	0.160	A
N-Channel Zero-Crossing Comparator		25	55	75	mA
OUT1 Maximum Output Current	2.6V ≤ V_{INP1} ≤ 5.5V (Note 2)	0.9			A
LX1 Leakage Current	V_{INP1} = 5.5V, LX1= GND or INP1, V_{OUT1} = 3.6V	-20	0.1	+20	µA
LX1 Duty-Cycle Range	V_{INP2} = 4.2V	0		100	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{INP1} = V_{INP2} = V_{INP3} = V_{IN} = 3.6V, V_{LBI} = 1.1V, V_{DBI} = 1.35V, $\overline{MR}$ = ON2 = IN, PGM3 = GND, circuit of Figure 1, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUT1 Discharge Resistance	V_{OUT1} = 3.3V, V_{DBI} = 1V		300 (Note 3)		Ω
SYNCHRONOUS BUCK REGULATOR 2 (REG2)					
FB2 Regulation Voltage	2.6V ≤ V_{INP2} ≤ 5.5V, load = 0 to 400mA	0.686	0.7	0.714	V
FB Input Current	V_{FB} = 0.7V		1	150	nA
Error-Amp Transconductance		150	250	350	µS
Dropout Voltage	Load = 400mA (Note 1)		150	250	mV
P-Channel On-Resistance	I_{LX2} = 180mA		0.25	0.4	Ω
	I_{LX2} = 180mA, V_{INP2} = 2.6V		0.3	0.5	
N-Channel On-Resistance	I_{LX2} = 180mA		0.2	0.35	Ω
Current-Sense Transresistance		0.40	0.47	0.54	V/A
P-Channel Current-Limit Threshold		1.15	1.275	1.45	A
P-Channel Pulse-Skipping Current Threshold		0.115	0.140	0.160	mA
N-Channel Zero-Crossing Comparator		25	55	75	mA
OUT2 Maximum Output Current	2.6V ≤ $V_{INP2\_}$ ≤ 5.5V (Note 2)	0.4			A
LX2 Leakage Current	V_{INP2} = 5.5V, LX2 = GND or INP2, V_{FB2} = 1V	-20	0.1	+20	µA
LX2 Duty-Cycle Range	$V_{INP\_}$ = 4.2V	0		100	%
LX2 Discharge Resistance	V_{LX2} = V_{DBI} = 1V		300		Ω
SYNCHRONOUS BUCK REGULATOR 3 (REG3)					
OUT3 Voltage Accuracy	PGM3 = GND, 3.6V ≤ $V_{INP3\_}$ ≤ 5.5V, load = 0 to 800mA	1.764	1.8	1.836	V
	PGM3 = REF, 3.6V ≤ $V_{INP3\_}$ ≤ 5.5V, load = 0 to 800mA	2.45	2.5	2.55	
	PGM3 = IN, 3.6V ≤ $V_{INP3\_}$ ≤ 5.5V, load = 0 to 800mA	3.234	3.3	3.366	
OUT3 Input Resistance	PGM3 = GND	340	650		kΩ
	PGM3 = REF	200	400		
	PGM3 = IN	160	320		
Error-Amp Transconductance	PGM3 = GND	105	175	245	µS
	PGM3 = REF	75	125	175	
	PGM3 = IN	55	95	135	
Dropout Voltage	Load = 800mA (Note 1)		220	400	mV
P-Channel On-Resistance	I_{LX3} = 180mA		0.25	0.4	Ω
	I_{LX3} = 180mA, V_{INP3} = 2.6V		0.3	0.5	
N-Channel On-Resistance	I_{LX3} = 180mA		0.2	0.35	Ω

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ELECTRICAL CHARACTERISTICS (continued)

(V_{INP1} = V_{INP2} = V_{INP3} = V_{IN} = 3.6V, V_{LBI} = 1.1V, V_{DBI} = 1.35V, $\overline{MR}$ = ON2 = IN, PGM3 = GND, circuit of Figure 1, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Transresistance		0.40	0.47	0.54	V/A
P-Channel Current-Limit Threshold		1.15	1.275	1.45	A
P-Channel Pulse-Skipping Current Threshold		0.115	0.140	0.160	A
N-Channel Zero-Crossing Comparator		25	55	75	mA
OUT3 Maximum Output Current	2.6V ≤ $V_{INP3\_}$ ≤ 5.5V (Note 2)	0.8			A
LX3 Leakage Current	V_{INP3} = 5.5V, LX3 = GND or INP3, V_{OUT3} = 3.6V	-20	0.1	+20	µA
LX3 Duty-Cycle Range	V_{INP3} = 4.2V	0		100	%
OUT3 Discharge Resistance	V_{OUT3} = 3.3V, V_{DBI} = 1V		300 (Note 3)		Ω
REFERENCE					
REF Output Voltage		1.225	1.25	1.275	V
REF Load Regulation	10µA < I_{REF} < 100µA		2.5	6.25	mV
REF Line Regulation	2.6V < V_{BATT} < 5.5V		0.6	5	mV
OSCILLATOR					
Switching Frequency		0.85	1	1.15	MHz
THERMAL SHUTDOWN					
Thermal Shutdown Temperature	T_J rising		160		°C
Thermal Shutdown Hysteresis			15		°C
SUPERVISORY/MANAGEMENT FUNCTIONS					
Reset Timeout	$\overline{MR}$ rising to $\overline{RSO}$ rising	55	65.5	75	ms
OUTOK Trip Threshold	V_{FB2} rising	94	95.5	97.5	%
	V_{FB2} falling	91	92.5	94	
OUTOK, $\overline{LBO}$ Minimum Assertion Time		107	126	145	µs
LBI Input Threshold	V_{LBI} falling	0.98	1.000	1.02	V
	V_{LBI} rising	1.00	1.020	1.04	
LBI Input Bias Current	V_{LBI} = 0.95V		0.02	0.1	µA
DBI Input Threshold	V_{DBI} falling, T_A = 0°C to +85°C	1.2103	1.235	1.2597	V
	V_{DBI} rising, T_A = 0°C to +85°C	1.2345	1.2597	1.2849	
	V_{DBI} falling, T_A = -40°C to +85°C	1.198	1.235	1.273	
	V_{DBI} rising, T_A = -40°C to +85°C	1.221	1.260	1.298	
DBI Input Bias Current	V_{DBI} = 1.25V		0.01	0.1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{INP1} = V_{INP2} = V_{INP3} = V_{IN} = 3.6V, V_{LBI} = 1.1V, V_{DBI} = 1.35V, $\overline{MR}$ = ON2 = IN, PGM3 = GND, circuit of Figure 1, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RSO}$, $\overline{LBO}$, OUTOK Output Low Level	2.6V ≤ $V_{IN\_}$ ≤ 5.5V, sinking 1mA			0.4	V
	$V_{IN\_}$ = 1V, sinking 100µA				
$\overline{RSO}$, $\overline{LBO}$, OUTOK Output High Leakage Current	$V_{\overline{RSO}}$ = $V_{\overline{LBO}}$ = V_{OUTOK} = 5.5V			0.1	µA
ON2, $\overline{MR}$, Input High Level	2.6V ≤ $V_{IN\_}$ ≤ 5.5V	1.6			V
ON2, $\overline{MR}$, Input Low Level	2.6V ≤ $V_{IN\_}$ ≤ 5.5V			0.4	V
ON2, $\overline{MR}$, PGM3, Input Leakage Current	V_{ON2} = $V_{\overline{MR}}$ = V_{PGM3} = GND, 5.5V	-1		+1	µA
PGM3 Selection Threshold	REG3 target = 1.8V, IN = 2.6V to 5.5V			0.4	V
	REG3 target = 2.5V, IN = 2.6V to 5.5V	1.1	REF	1.4	
	REG3 target = 3.3V, IN = 2.6V to 5.5V	$V_{IN\_}$ - 0.25			

Note 1: Dropout voltage is not tested. Guaranteed by P-channel switch resistance and assumes a 72mΩ (REG1 and REG3) or 162mΩ (REG2) maximum ESR of inductor.

Note 2: The maximum output current is guaranteed by the following equation:

$$I_{OUT(MAX)} = \frac{I_{LIM} - \frac{V_{OUT}(1-D)}{2 \times f \times L}}{1 + (R_N + R_L)\frac{(1-D)}{2 \times f \times L}}$$

where:

$$D = \frac{V_{OUT} + I_{OUT(MAX)}(R_N + R_L)}{V_{IN} + I_{OUT(MAX)}(R_N + R_P)}$$

and:
R_N = N-channel synchronous rectifier R_{DSON}
R_P = P-channel power switch R_{DSON}
R_L = external inductor ESR
$I_{OUT(MAX)}$ = maximum required load current
f = operating frequency minimum
L = external inductor value

Note 3: Specified resistance is in series with an internal diode to LX2.

Note 4: Specifications to -40°C are guaranteed by design and not production tested.

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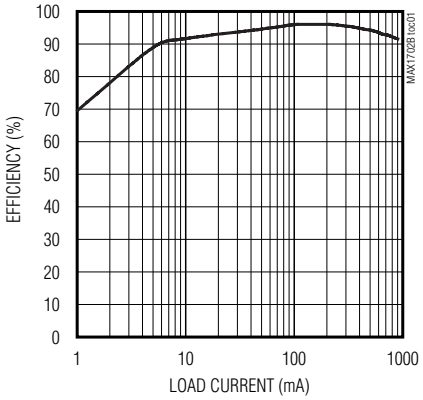
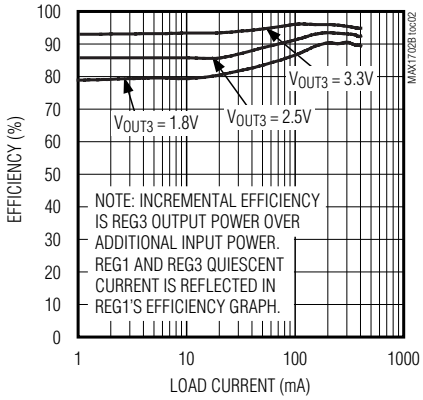
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

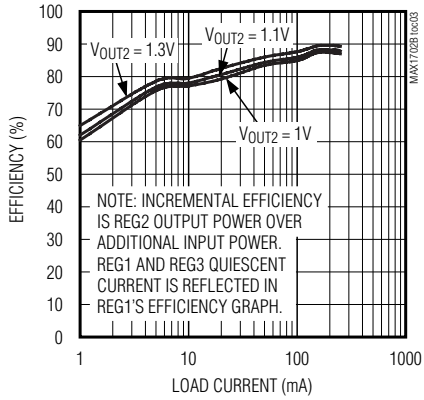
REG1 EFFICIENCY vs. LOAD CURRENT



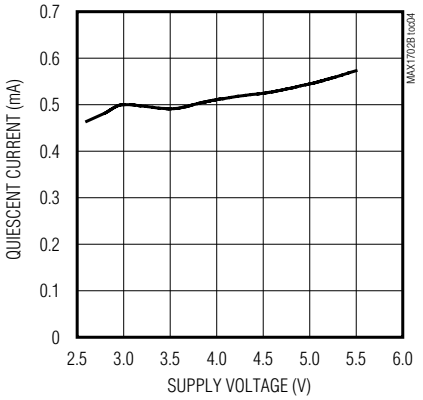
REG3 INCREMENTAL EFFICIENCY vs. LOAD CURRENT



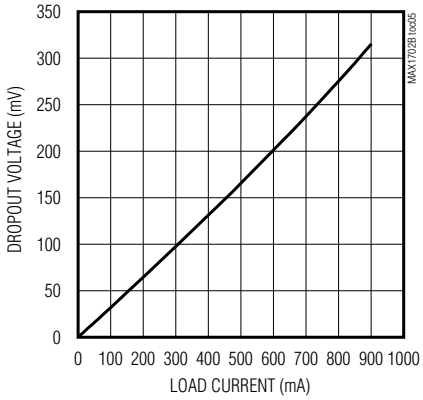
REG2 INCREMENTAL EFFICIENCY vs. LOAD CURRENT



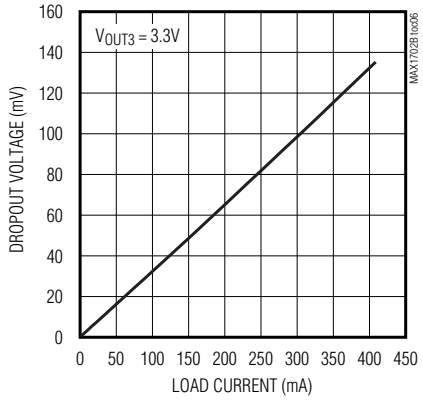
NO LOAD QUIESECNT CURRENT vs. SUPPLY VOLTAGE



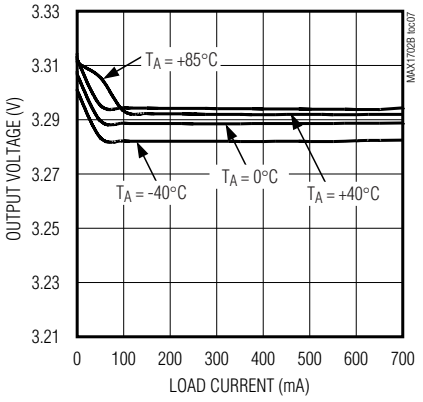
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT (V_{IN} = 3.3V)



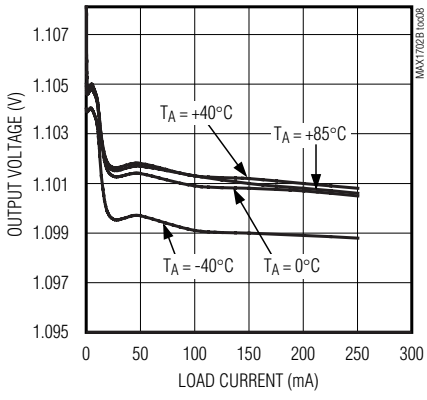
REG3 DROPOUT VOLTAGE vs. LOAD CURRENT (V_{IN} = 3.3V)



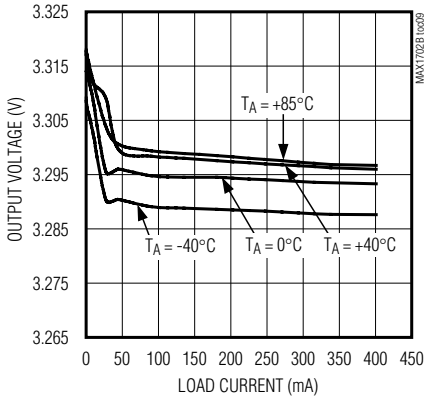
REG1 OUTPUT VOLTAGE vs. LOAD CURRENT



REG2 OUTPUT VOLTAGE vs. LOAD CURRENT



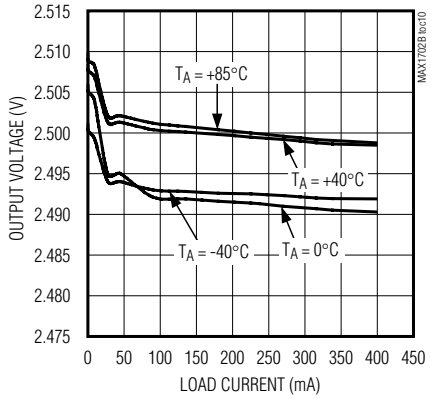
REG3 OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT3} = 3.3V)



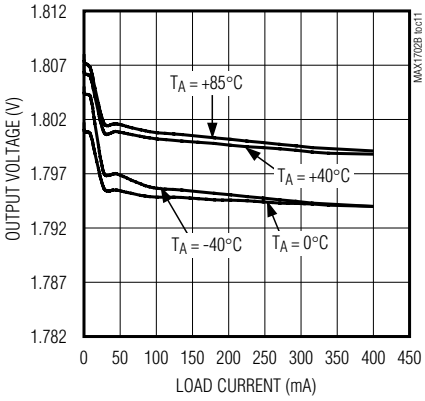
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

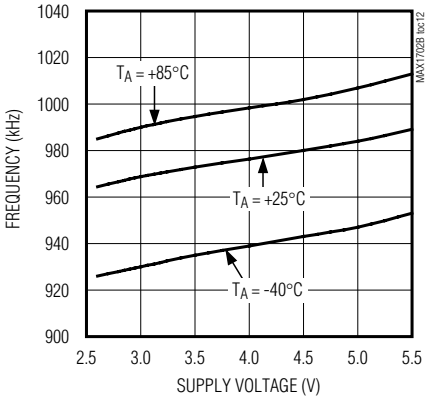
REG3 OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT3} = 2.5V)



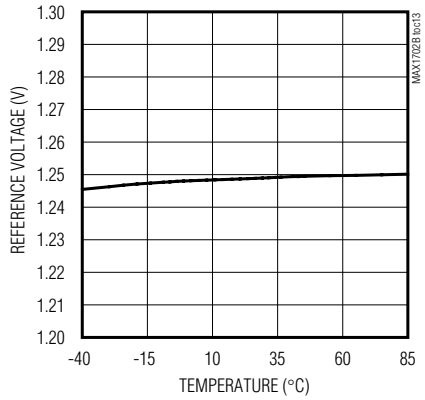
REG3 OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT3} = 1.8V)



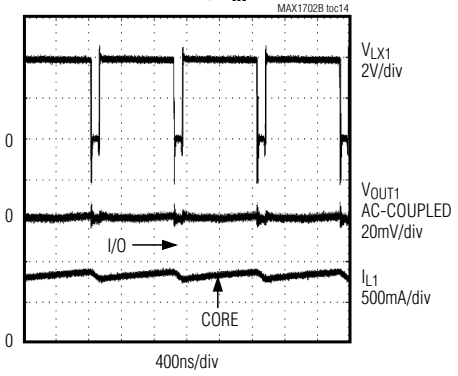
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



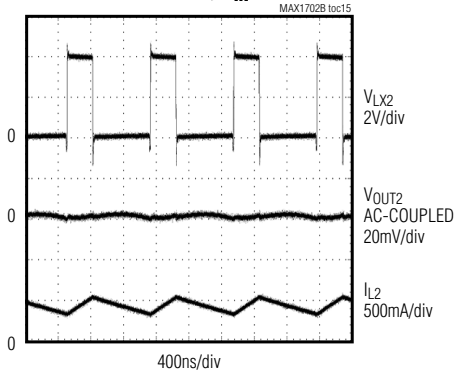
INTERNAL REFERENCE vs. TEMPERATURE



REG1 HEAVY-LOAD SWITCHING WAVEFORM LOAD = 800mA, V_{IN} = 4V



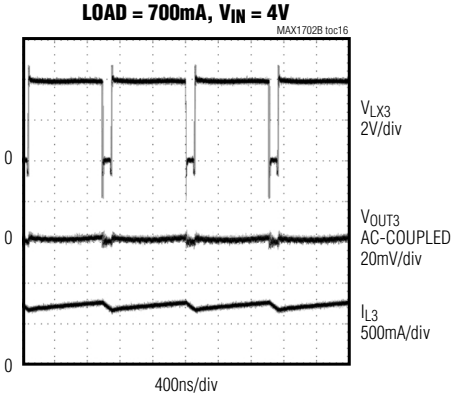
REG2 HEAVY-LOAD SWITCHING WAVEFORM LOAD = 400mA, V_{IN} = 4V



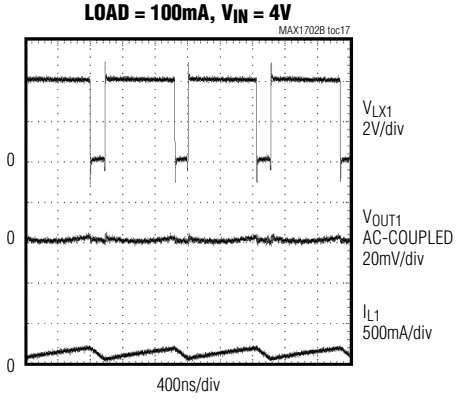
Triple-Output Power-Management IC for Microprocessor-Based Systems

Typical Operating Characteristics (continued)

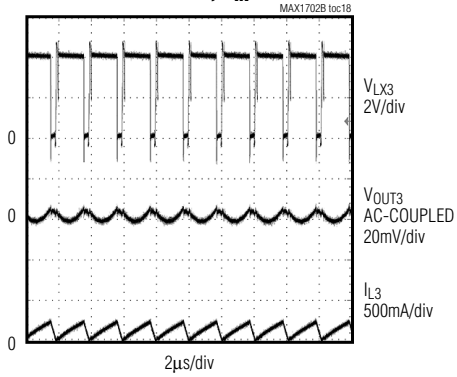
REG3 HEAVY-LOAD SWITCHING WAVEFORM
LOAD = 700mA, V_{IN} = 4V



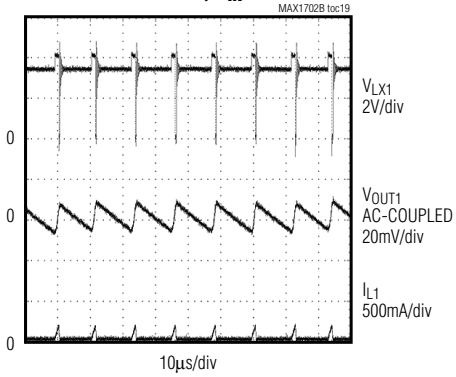
REG1 MEDIUM-LOAD SWITCHING WAVEFORM
LOAD = 100mA, V_{IN} = 4V



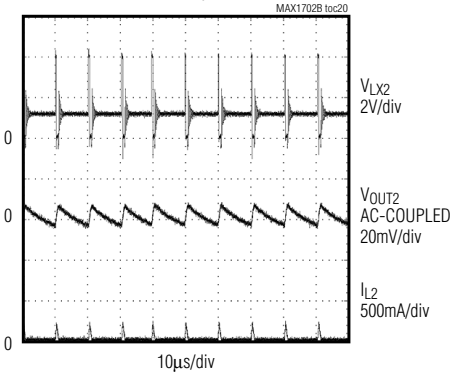
REG3 MEDIUM-LOAD SWITCHING WAVEFORM
LOAD = 100mA, V_{IN} = 4V



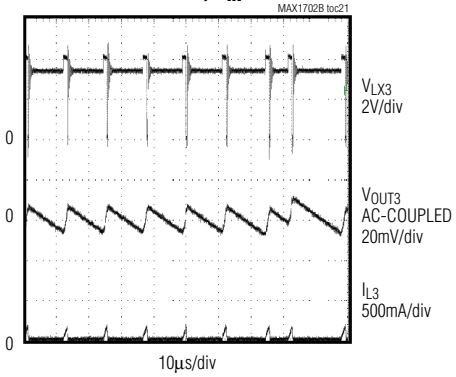
REG1 LIGHT-LOAD SWITCHING WAVEFORM
LOAD = 10mA, V_{IN} = 4V



REG2 LIGHT-LOAD SWITCHING WAVEFORM
LOAD = 10mA, V_{IN} = 4V



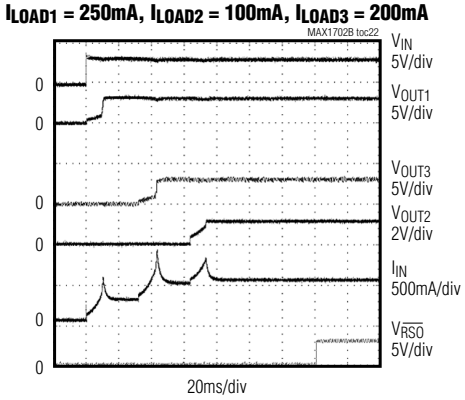
REG3 LIGHT-LOAD SWITCHING WAVEFORM
LOAD = 10mA, V_{IN} = 4V



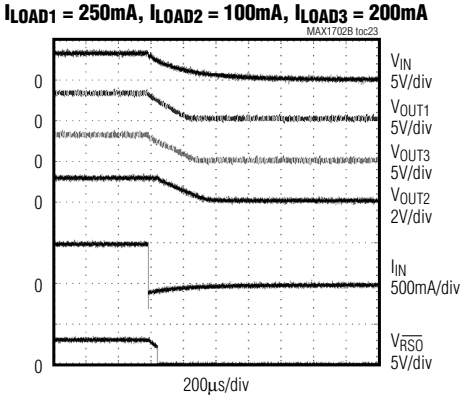
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

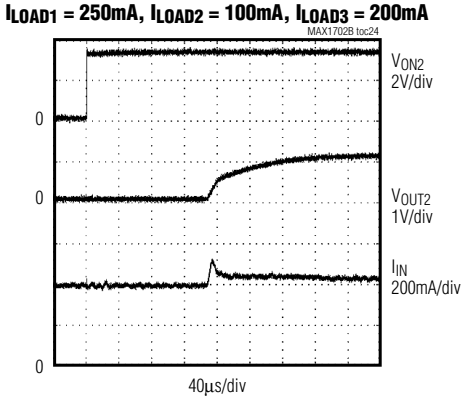
TURN-ON SEQUENCE FROM POWER APPLICATION
I_{LOAD1} = 250mA, I_{LOAD2} = 100mA, I_{LOAD3} = 200mA



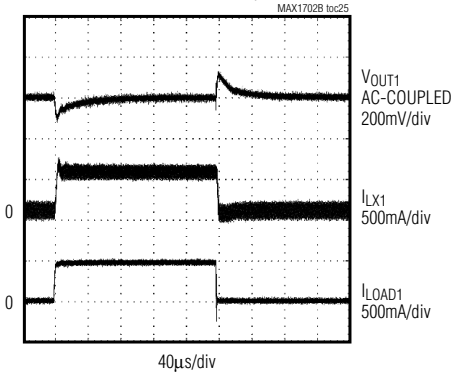
TURN-OFF SEQUENCE
I_{LOAD1} = 250mA, I_{LOAD2} = 100mA, I_{LOAD3} = 200mA



TURN-ON DELAY
I_{LOAD1} = 250mA, I_{LOAD2} = 100mA, I_{LOAD3} = 200mA



REG1 LOAD TRANSIENT WAVEFORM
LOAD = 100mA TO 500mA, V_{IN} = 4V

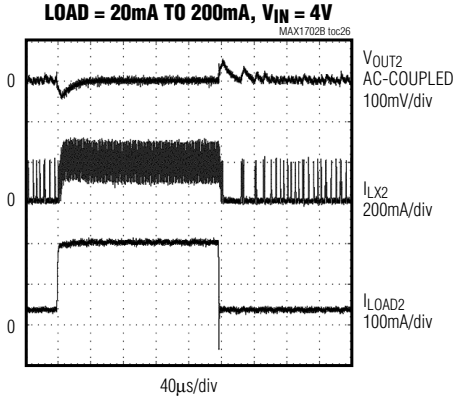


Triple-Output Power-Management IC for Microprocessor-Based Systems

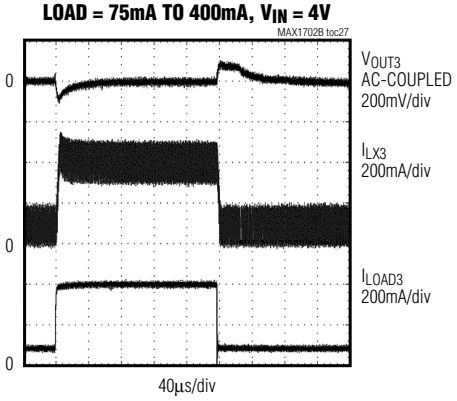
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

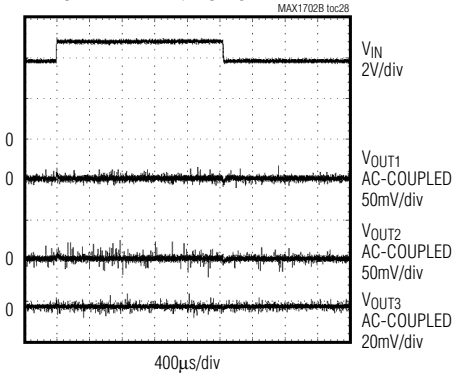
REG2 LOAD TRANSIENT WAVEFORM
LOAD = 20mA TO 200mA, V_{IN} = 4V



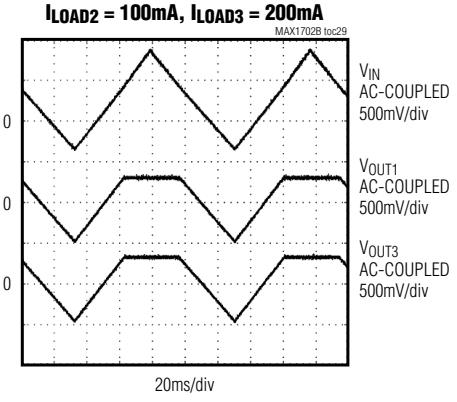
REG3 LOAD TRANSIENT WAVEFORM
LOAD = 75mA TO 400mA, V_{IN} = 4V



LINE TRANSIENT RESPONSE WAVEFORM
V_{IN} = 4V TO 5V, I_{LOAD1} = 250mA,
I_{LOAD2} = 100mA, I_{LOAD3} = 200mA



ENTERING AND EXITING DROPOUT WAVEFORM
V_{IN} = 2.75V TO 4V, I_{LOAD1} = 250mA,
I_{LOAD2} = 100mA, I_{LOAD3} = 200mA



Pin Description

PIN	NAME	FUNCTION
1, 9, 13, 18, 19, 26, 27, 31, 35	N.C.	No Connection. These pins are not internally connected.
2	LBI	Low-Battery Input. Connect a resistive voltage-divider from the battery voltage to LBI to set the low-battery threshold. LBI threshold voltage is 1.235V.
3	DBI	Dead-Battery Input. Connect a resistive voltage-divider from the battery voltage to DBI to set the dead-battery voltage threshold. When the voltage at DBI is below the 1.25V threshold, the MAX1702B is turned off and draws only 5µA from the battery.
4	ON2	REG2 On/Off Input. Drive ON2 high to turn on REG2, drive it low to turn it off. When enabled, the MAX1702B soft-starts REG2, when disabled, the output of REG2 is internally discharged to PG2.
5	PGM3	REG3 Regulation Voltage-Control Input. Connect PGM3 to IN, REF, or GND to set the REG3 output regulation voltage. Connect PGM3 to GND for 1.8V, REF for 2.5V, and IN for 3.3V.
6	GND	Connect Pin 6 to Pin 8
7	REF	Reference Output. Output of the 1.25V reference. Bypass REF to GND with a 0.1µF or greater capacitor.
8	GND	Analog Ground. Connect GND to a local analog ground plane with no high-current paths. GND should be connected to the main ground plane at a single point as close to the IC and the IN bypass capacitor as possible. Connect the ground of the low-noise components, such as resistive voltage-dividers and reference bypass capacitor to the analog ground plane.
10	IN	Analog Supply Input. Bypass IN to GND with a 1µF or greater low-ESR capacitor.
11	$\overline{RSO}$	Reset Output. $\overline{RSO}$ is low (sinks current to GND) during initial startup or while the manual reset input, $\overline{MR}$, is asserted. $\overline{RSO}$ remains low for 65.5ms after all regulators are in regulation or after $\overline{MR}$ is deasserted. $\overline{RSO}$ is an open-drain output. RSO remains high when REG2 is turned off. The $\overline{RSO}$ line maintains a valid low output for IN as low as 1V.
12	PG1	REG1 Power Ground. Connect PG1 directly to a power ground plane. Connect PG1, PG2, PG3 and GND together at a single point as close to the IC as possible.
14	LX1	REG1 Power-Switching Node. Connect the external inductor of the REG1 output LC filter from LX1 to OUT1 (see the *Inductor Selection* section).
15	INP1	REG1 Power Input. Bypass INP1 to PG1 with a 1.0µF or greater low-ESR capacitor. INP1, INP2, INP3, and IN must be connected together externally. A single 4.7µF capacitor can be used for INP1, INP2, and INP3.
16	$\overline{MR}$	Manual Reset Input. A momentary low on $\overline{MR}$ forces $\overline{RSO}$ to go low. $\overline{RSO}$ remains low as long as $\overline{MR}$ is low, and returns high 65.5ms after $\overline{MR}$ returns high and all output voltages are in regulation.
17	COMP1	REG1 Compensation Node. Connect a series resistor and capacitor from COMP1 to GND in parallel with a 33pF capacitor to compensate REG1 (see the *Compensation and Stability* section).

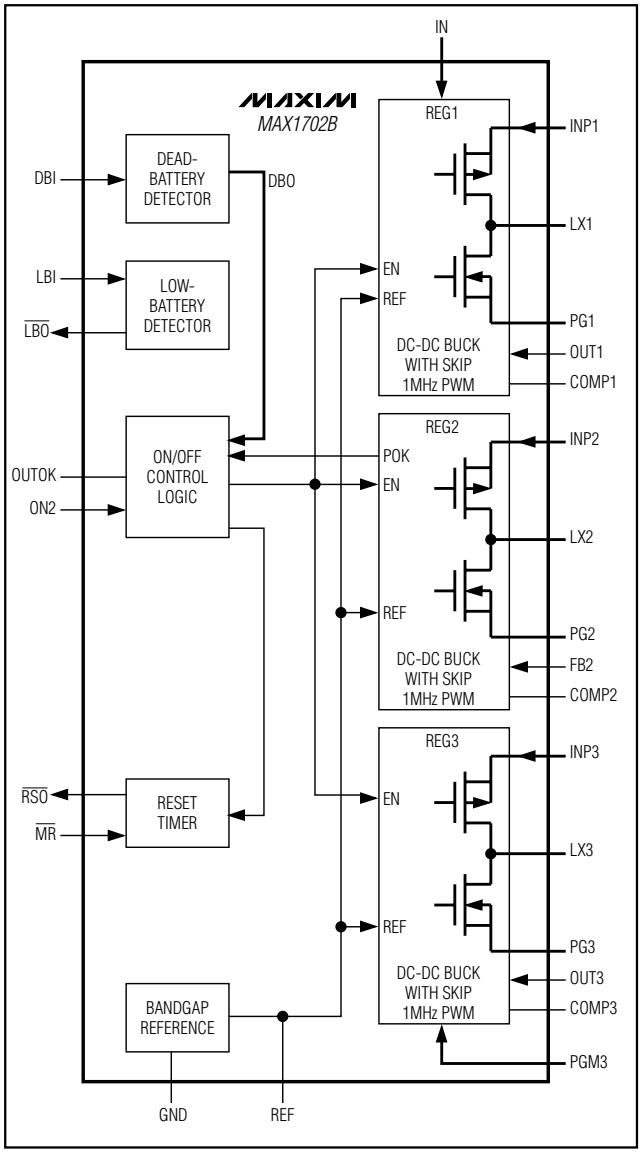
Triple-Output Power-Management IC for Microprocessor-Based Systems

Pin Description (continued)

PIN	NAME	FUNCTION
20	OUT1	REG1 Output-Voltage Sense Input. Bypass OUT1 to PG1 with a 10µF or greater low-ESR capacitor (see the *Output Capacitor Selection* section).
21	COMP2	REG2 Compensation Node. Connect a series resistor and capacitor from COMP2 to GND in parallel with a 33pF capacitor to compensate REG2 (see the *Compensation and Stability* section).
22	OUTOK	Output-OK Output. OUTOK sinks current to GND when the voltage at REG2 is below the regulation threshold. When the output is in regulation, OUTOK is high impedance. OUTOK is used by the processor to indicate when it is safe for the processor to exit sleep mode. OUTOK is an open-drain output. OUTOK maintains a valid low output for IN as low as 1V.
23	PG2	REG2 Power Ground. Connect PG2 directly to a power ground plane. Connect PG1, PG2, PG3, and GND together at a single point as close to the IC as possible.
24	LX2	REG2 Power-Switching Node. Connect the external inductor of the REG2 output LC filter from LX2 to OUT2. LX2 discharges OUT2 when REG2 is disabled (see the *Inductor Selection* section).
25	INP2	REG2 Power Input. Bypass INP2 to PG2 with a 1.0µF or greater low-ESR capacitor. INP1, INP2, INP3, and IN must be connected together externally. A single 4.7µF capacitor can be used for INP1, INP2, and INP3.
28	FB2	REG2 Feedback-Sense Input. Set the REG2 output voltage with a resistive voltage-divider from the REG2 output voltage to FB2. The FB2 regulation threshold is 0.7V. Connect FB2 directly to OUT2 for an output voltage of 0.7V.
29	OUT3	REG3 Output-Voltage Sense Input. Bypass OUT3 to GND with a 10µF or greater low-ESR capacitor (see the *Output Capacitor Selection* section).
30	COMP3	REG3 Compensation Node. Connect a series resistor and capacitor from COMP3 to GND in parallel with a 33pF capacitor to compensate REG3 (see the *Compensation and Stability* section).
32	PG3	REG3 Power Ground. Connect PG3 directly to a power ground plane. Connect PG1, PG2, PG3, and GND together at a single point as close to the IC as possible.
33	LX3	REG3 Power-Switching Node. Connect the external inductor of the REG3 output LC filter from LX3 to OUT3 (see the *Inductor Selection* section).
34	INP3	REG3 Power Input. Bypass INP3 to PG3 with a 1.0µF or greater low-ESR capacitor. INP1, INP2, INP3, and IN must be connected together externally. A single 4.7µF capacitor can be used for INP1, INP2, and INP3.
36	$\overline{LBO}$	Low-Battery Output. $\overline{LBO}$ sinks current to GND when the voltage at LBI is below the LBI threshold voltage; $\overline{LBO}$ is high impedance when LBI is above the threshold. $\overline{LBO}$ is an open-drain output. $\overline{LBO}$ maintains a valid low output level for IN as low as 1V.

Triple-Output Power-Management IC for Microprocessor-Based Systems

Functional Diagram



Detailed Description

The MAX1702B triple-output step-down DC-DC converter is ideal for powering PDA, palmtop, and subnotebook computers. Normally, these devices require separate power supplies for the processor core, memory, and the peripheral circuitry. The MAX1702B's REG1 provides a fixed 3.3V output designed to power the microprocessor I/O and other peripheral circuitry. REG1 delivers up to 900mA output current. The microprocessor core is powered from REG2, which has an adjustable 0.7V to V_{IN} output, providing up to 400mA output current. The third output, REG3, is designed to power memory. REG3 output voltage is set to one of 3 voltages; 3.3V (PGM3 = IN), 2.5V (PGM3 = REF), or 1.8V (PGM3 = GND) and delivers up to 800mA of output current. All three regulators utilize a proprietary regulation scheme allowing PWM operation at medium to heavy loads, and automatically switch to pulse skipping at light loads for improved efficiency. Under low-battery conditions, the MAX1702B issues a warning ($\overline{LBO}$ output).

The MAX1702B employs PWM control at medium and heavy loads, and skip mode at light loads (below approximately 80mA) to improve efficiency and reduce quiescent current to 485µA. During skip operation, the MAX1702B switches only as needed to service the load, reducing the switching frequency and associated losses in the internal switch, the synchronous rectifier, and the external inductor.

There are three steady-state operating conditions for the MAX1702B. The device performs in continuous conduction for heavy loads. The inductor current becomes discontinuous at light loads, requiring the synchronous rectifier to be turned off before the end of a cycle as the inductor current reaches zero. The device enters into skip mode when the converter output voltage exceeds its regulation limit before the inductor current reaches the pulse-skip threshold.

During skip mode, a switching cycle initiates when the output voltage drops below the regulation voltage. The P-channel MOSFET switch turns on and conducts current to the output-filter capacitor and load until the inductor current reaches the pulse-skip current threshold. Then the main switch turns off, and the current flows through the synchronous rectifier to the output-filter capacitor and the load. The synchronous rectifier is turned off when the inductor current approaches zero. The MAX1702B waits until the output voltage drops below the regulation voltage again to initiate the next cycle.

100% Duty-Cycle Operation

If the inductor current does not rise sufficiently to supply the load during the on-time, the switch remains on, allowing operation up to 100% duty cycle. This allows the output voltage to maintain regulation while the input voltage approaches the regulation voltage. Dropout voltage is the output current multiplied by the on-resistance of the internal switch and inductor, approximately 220mV for an 800mA load for REG1 and REG3 and 150mV for a 400mA load on REG2.

Near dropout, the on-time may exceed one PWM clock cycle; therefore, small amplitude subharmonic ripple can occur in the output voltage. During dropout, the

Triple-Output Power-Management IC for Microprocessor-Based Systems

high-side P-channel MOSFET turns on, and the controller enters a low-current consumption mode. The device remains in this mode until the MAX1702B is no longer in dropout.

Synchronous Rectification

An N-channel synchronous rectifier eliminates the need for an external Schottky diode and improves efficiency. The synchronous rectifier turns on during the second half of each cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current falls. The synchronous rectifier is turned off at the end of the cycle (at which time another on-time begins) or when the inductor current approaches zero.

Battery Monitoring and Undervoltage Lockout

The MAX1702B does not operate with input voltages below the undervoltage lockout (UVLO) threshold of 2.35V (typ). The inputs remain high impedance until the supply voltage exceeds the UVLO threshold, reducing battery load under this condition.

The MAX1702B provides a low-battery comparator that compares the voltage on LBI to the reference voltage. An open-drain output ($\overline{LBO}$) goes low when the LBI voltage is below 1V. Use a resistive voltage-divider network as shown in Figure 1 to set the trip voltage to the desired level. $\overline{LBO}$ is high impedance in shutdown mode.

The MAX1702B also provides a dead-battery comparator that turns off the IC when the battery has excessively discharged. When the voltage at DBI is below the 1.235V threshold, the MAX1702B is turned off and draws only 5µA from the battery. Use a resistive voltage-divider network as shown in Figure 1 to set the trip voltage to the desired level.

Power-On Sequencing

The MAX1702B starts when the input voltage rises above the UVLO threshold and the voltage at DBI is greater than the DBI threshold. When power is initially applied, REG1 starts in soft-start mode. Once OUT1 reaches its regulation voltage, REG3 ramps to its target in soft-start mode. Finally, once OUT3 reaches its regulation voltage, REG2 ramps to its target in soft-start mode. The $\overline{RSO}$ output holds low during this time and remains low until 65.5ms after REG2 reaches its target output voltage.

Once all the regulators are running, ON2 turns REG2 on and off. During startup (before the end of the reset period) REG2 is enabled and can only be turned off once the $\overline{RSO}$ output goes high. When turned off, the REG2 output voltage is discharged to PG2 through LX2.

REG1 and REG3 Step-Down Converters

REG1 and REG3 are 1MHz PWM, current-mode step-down converters and generate 3.3V at up to 900mA (REG1), and 3.3V, 2.5V, or 1.8V at up to 800mA (REG3). Internal switches and synchronous rectifiers are integrated for small size and improved efficiency. Both regulators remain on while the input voltage is above the UVLO threshold and DBI is above the DBI threshold. REG1 and REG3 cannot be independently turned on or off. To turn both regulators off, pull DBI below the DBI threshold (1.235V typ).

The REG3 output voltage is set through the PGM3 pin. Connect PGM3 to IN to set the output voltage to 3.3V, connect it to REF to set it to 2.5V, and connect it to GND to set the voltage to 1.8V.

REG2 Step-Down Converter

REG2 is a 1MHz, current-mode step-down converter and generates a 0.7V to V_{IN} output delivering up to 400mA. An internal switch and synchronous rectifier are used for small size and improved efficiency. REG2 is turned on and off through the ON2 input. Drive ON2 low to turn off the regulator, and high to turn it on. OUTOK goes low when the REG2 output voltage drops below 92.5% of the regulation voltage. OUTOK is an open-drain output. OUTOK can be used to signal the processor that the REG2 voltage is in, allowing the processor to exit from sleep mode into run mode.

Reset Output

MAX1702B features an active-low, open-drain reset output ($\overline{RSO}$), $\overline{RSO}$ holds low during startup or when the manual reset input $\overline{MR}$ is held low. $\overline{RSO}$ goes high impedance 65.5ms after REG2 reaches its target value and the $\overline{MR}$ input goes high. (see the *Power-On Sequencing* section). Note that RSO remains high when REG2 is turned off.

Applications Information

Setting the Output Voltages

The REG1 output voltage is fixed at 3.3V and cannot be changed. The REG3 output voltage can be set by the PGM3 input to either 3.3V (connect PGM3 to IN), 2.5V (connect PGM3 to REF), or 1.8V (connect PGM3 to GND). The REG2 output voltage is set between 0.70V and V_{IN} through a resistive voltage-divider from the REG2 output voltage to FB2 (Figure 1).

Select feedback resistor R5 to be less than 14kΩ. R4 is then given by:

$$R4 = R5\left(\frac{V_{OUT}}{V_{FB2}} - 1\right)$$

where V_{FB2} = 0.70V and V_{OUT} is the REG2 output voltage.

Compensation and Stability

Compensate each regulator by placing a resistor and a capacitor in series, from COMP_ to GND and connect a 33pF capacitor from COMP_ to GND for improved noise immunity (Figure 1). The capacitor integrates the current from the transconductance amplifier, averaging output-voltage ripple. This sets the device speed for transient responses and allows the use of small ceramic output capacitors. The resistor sets the proportional gain of the output error voltage by a factor $g_m \times R_C$. Increasing this resistor also increases the sensitivity of the control loop to the output-voltage ripple.

This resistor and capacitor set a compensation zero that defines the system's transient response. The load pole is a dynamic pole, shifting frequency with changes in load. As the load decreases, the pole frequency shifts lower. System stability requires that the compensation zero must be placed properly to ensure adequate phase margin (at least 30°). The following is a design procedure for the compensation network:

1) Select an appropriate converter bandwidth (f_C) to stabilize the system while maximizing transient response. This bandwidth should not exceed 1/5 of the switching frequency. Use 100kHz as a reasonable starting point.
2) Calculate the compensation capacitor, COMP_, based on this bandwidth. Calculate COMP1 and COMP3 with the following equation:

$$C_{COMP1/3} = \left(\frac{V_{OUT(MAX)}}{I_{OUT(MAX)}}\right)\left(\frac{1}{R_{CS}}\right)\left(\frac{1}{2\times\pi\times f}\right)g_m$$

where RCS is the regulator's current-sense transresistance and gm is the regulators error amplifier transconductance. Calculate COMP2 with the following equation:

$$C_{COMP2} = \left(\frac{V_{OUT(MAX)}}{I_{OUT(MAX)}}\right)\left(\frac{1}{R_{CS}}\right)\left(\frac{1}{2\times\pi\times f}\right)\left(g_m \times \frac{R5}{R4+R5}\right)$$

where R_{CS} is REG2's current-sense transresistance and g_m is REG2's error-amplifier transconductance.

Calculate the equivalent load impedance, R_L, by:

$$R_L = \frac{V_{OUT(MIN)}}{I_{OUT(MAX)}}$$

where $V_{OUT(MIN)}$ equals the minimum output voltage. $I_{OUT(MAX)}$ equals the maximum load current. Choose the output capacitor, C_{OUT} (see the *Output Capacitor Selection* section). Calculate the compensation resistance (R_C) value to cancel out the dominant pole created by the output load and the output capacitance:

$$\frac{1}{2\times\pi\times R_L\times C_{OUT}} = \frac{1}{2\times\pi\times RC\times C_{COMP\_}}$$

Solving for R_C gives:

$$R_C = \frac{R_L\times C_{OUT}}{C_{COMP\_}}$$

To find $C_{COMPHF\_}$, calculate the high-frequency compensation pole to cancel the zero created by the output capacitor's equivalent series resistance (ESR):

$$\frac{1}{2\times\pi\times R_{ESR}\times C_{OUT}} = \frac{1}{2\times\pi\times R_C\times C_{COMPHF\_}}$$

Solving for $C_{COMPHF\_}$ gives:

$$C_{COMPHF\_} = \frac{R_{ESR}\times C_{OUT}}{R_C}, \text{but not less than 33pF}$$

If low-ESR ceramic capacitors are used, the $C_{COMPHF\_}$ equation can yield a very small capacitance value. In such cases, do not use less than 33pF to maintain noise immunity.

Inductor Selection

A 4.7µH inductor with a saturation current of at least 1.5A is recommended for most applications. For best efficiency, use an inductor with low ESR. See Table 1 for recommended inductors and manufacturers. For most designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation:

$$L_{IDEAL} = \frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}\times LIR\times I_{OUT(MAX)}\times f_{OSC}}$$

where LIR is the inductor current ripple as a percentage of the load current.

LIR should be kept between 20% and 40% of the maximum load current for best performance and stability. The maximum inductor current is:

$$I_{LMAX} = \left(1+\frac{LIR}{2}\right) I_{OUT(MAX)}$$

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Table 1. Suggested Inductors

MANUFACTURER	PART NUMBER	INDUCTANCE (µH)	ESR (mW)	SATURATION CURRENT (A)	DIMENSIONS (mm)
Coilcraft	DO1606	4.7	120	1.2	5.3 x 5.3 x 2
Coilcraft	LPT1606-472	4.7	240 (max)	1.2	6.5 x 5.3 x 2.0
Sumida	CDRH4D28-4R7	4.7	56	1.32	4.6 x 5 x 3
Sumida	CDRH5D18-4R1	4.1	57	1.95	5.5 x 5.5 x 2
Sumida	CR43	4.7	108.7	1.15	4.5 x 4 x 3.5

The inductor current becomes discontinuous if I_{OUT} decreases to LIR/2 from the output current value used to determine L_{IDEAL}.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source but instead are shunted through the input capacitor.

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. The input capacitor RMS current is:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}}\right)$$

Output Capacitor Selection

The output capacitor is required to keep the output-voltage ripple small and to ensure regulation control-loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors are recommended. The output ripple is approximately:

$$V_{RIPPLE} \approx LIR \times I_{OUT(MAX)} \times \left[ESR + \frac{1}{2 \times f_{OSC} \times C_{OUT}}\right]$$

See the *Compensation and Stability* section for a discussion of the influence of output capacitance and ESR on regulation control-loop stability.

The capacitor voltage rating must exceed the maximum applied capacitor voltage. Consult the manufacturer's specifications for proper capacitor derating. Avoid Y5V and Z5U dielectric types due to their huge voltage and temperature coefficients of capacitance and ESR. X7R and X5R dielectric types are recommended.

Setting the Battery Detectors

The low-battery and dead-battery detector trip points can be set by adjusting the resistor values of the divider string (R1, R2, and R3) in Figure 1 according to the following:

1) Choose R3 to be less than 250kΩ
2) $R1 = R3 \times V_{BL} \times (1 - V_{TH}/V_{BD})$
3) $R2 = R3 \times (V_{TH} \times V_{BL}/V_{BD} - 1)$

where V_{BL} is the low-battery voltage, V_{BD} is the dead-battery voltage, and V_{TH} = 1.235V.

PC Board Layout and Routing

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible, and keep their traces short, direct, and wide. Connect their ground pins to a single common power ground plane. The external voltage-feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces (from the LX pin, for example) away from the voltage-feedback network; also, keep them separate, using grounded copper. Connect GND and PG_ pins together at a single point, as close as possible to the MAX1702B. Refer to the MAX1702B evaluation kit for a PC board layout example.

Chip Information

TRANSISTOR COUNT: 10,890

PROCESS: BiCMOS

Typical Operating Circuit

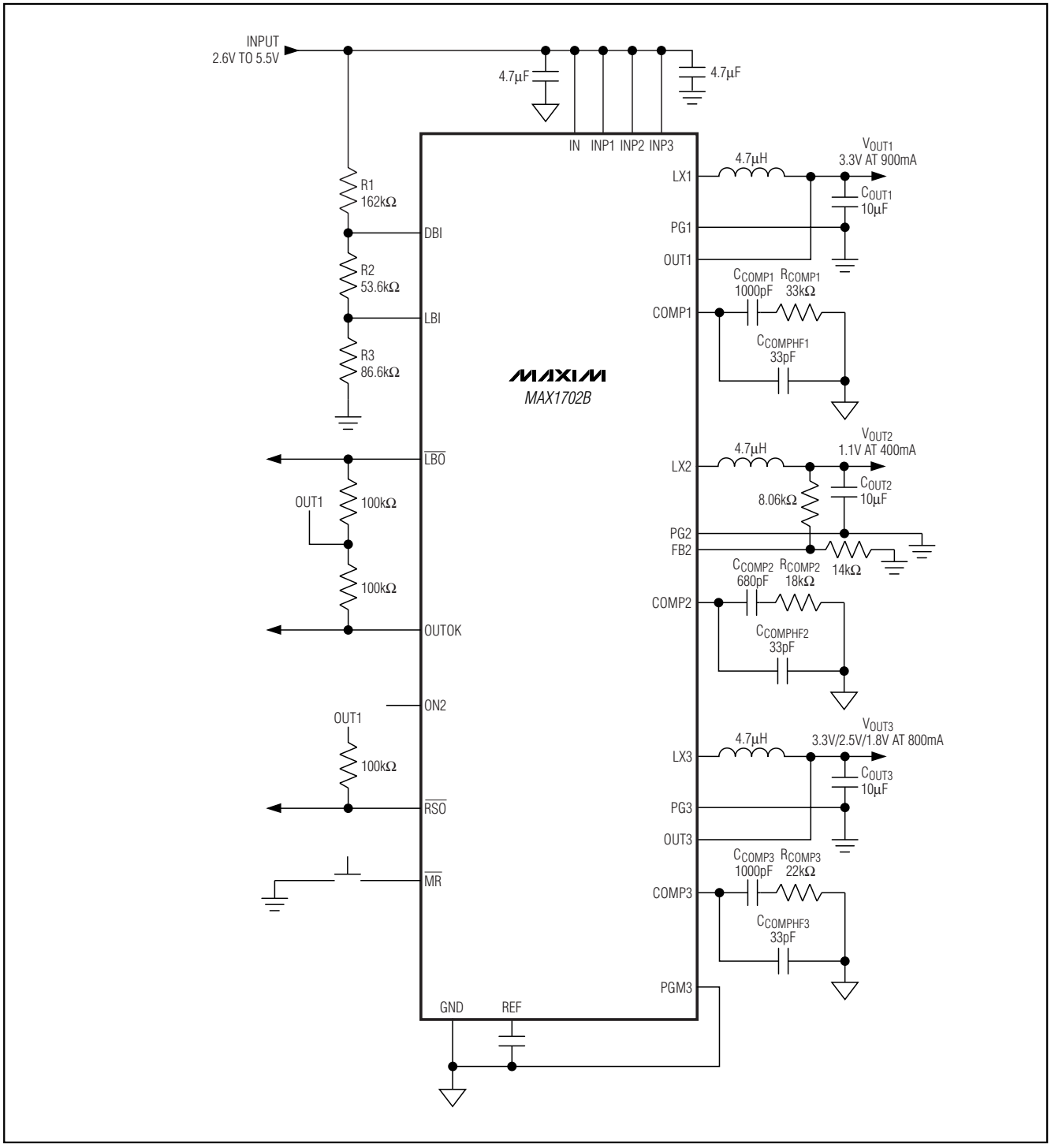
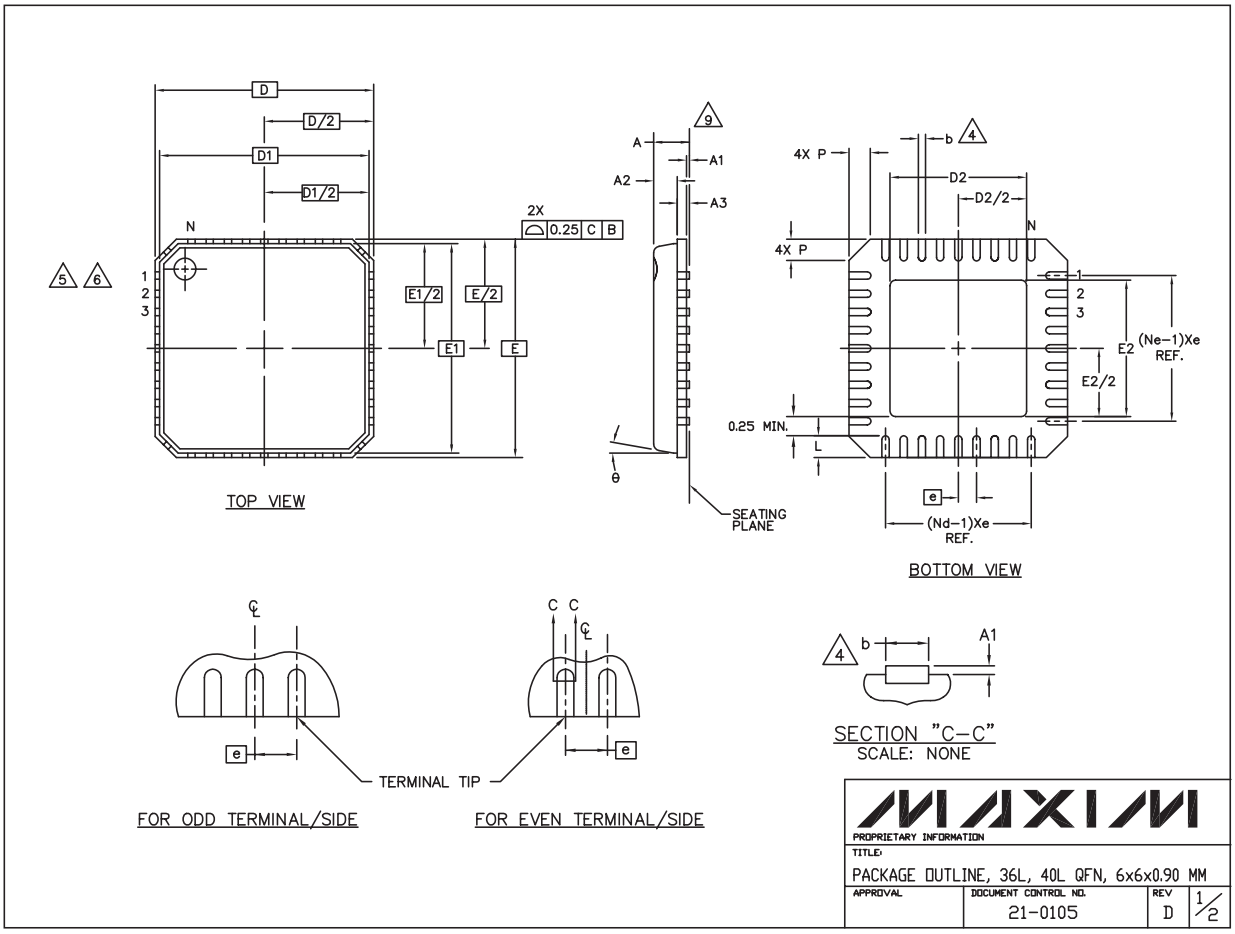


Figure 1. Typical Operating Circuit

Triple-Output Power-Management IC for Microprocessor-Based Systems

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		6.00 BSC		
D1		5.75 BSC		
E		6.00 BSC		
E1		5.75 BSC		
θ	0°		12°	
P	0		0.60	
D2	1.75		4.25	
E2	1.75		4.25	

SYMBOL	PITCH VARIATION C						
	MIN.	NOM.	MAX.	NOTE	MIN.	NOM.	MAX.
e	0.50 BSC				0.50 BSC		
N	36			3	40		
Nd	9			3	10		
Ne	9			3	10		
L	0.50	0.60	0.75		0.30	0.40	0.50
b	0.18	0.23	0.30	4	0.18	0.23	0.30

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 36L, 40L QFN, 6x6x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0105	D	2/2